AMENDMENTS IN THE CLAIMS

1. (currently amended) A data transmission system comprising:

a hub including a plurality of adapters including at least a requesting adapter and at least a destination adapter, wherein each of said plurality of adapters further includes:

a clock multiplier for multiplying by sixteen a data clock of the system and providing control logic with timing pulses used to transmit thirty-two bits of a request signal;

a plurality of data processing systems, including at least a requesting data processing system and at least a destination data processing system, coupled to said hub via said requesting adapter and said destination adapter; and

a crossbar switch coupling said plurality of adapters, wherein said requesting data processing system transmits at least a data frame to said destination adapter, said requesting adapter converts said data frame into concatenated slots of an identical size and transmits ~~said data frame~~ said concatenated slots of said identical size through said crossbar switch.

2. (previously presented) The data transmission system according to Claim 1, wherein said plurality of data processing systems is a plurality of local area networks (LANs), including at least a requesting LAN and at least a destination LAN.

3. (previously presented) The data transmission system according to Claim 1, wherein said plurality of adapters is a plurality of local area network (LAN) adapters, including at least a requesting LAN adapter and at least a destination LAN adapter.

4. (previously presented) The data transmission system according to Claim 1, wherein said data frame is a LAN data frame.

5. (previously presented) The data transmission system according to Claim 1, wherein said crossbar switch is an asynchronous transfer mode (ATM) crossbar switch.

6. (previously presented) The data transmission system according the Claim 1, said plurality of LAN adapter further includes:

a control logic for transmitting a plurality of request signals (REQ) to said crossbar switch, each of said plurality of requests signals associated with said destination adapter.

7. (currently amended) The data transmission system according to Claim 1, said crossbar switch further comprises:

a scheduler for transmitting a plurality of grant signals (GNT) associated with ~~said~~ a plurality of request signals enabling said requesting data processing system to transmit at least said data frame to said destination data processing system, said plurality of grant signals being transmitted in an order depending upon a predetermined algorithm controlling said scheduler regardless the order said plurality of requests are transmitted by said requesting adapter.

8. (previously presented) The data transmission system according to Claim 1, wherein said requesting adapter further comprises:

a serial communication controller further including:

a means for converting said data frame received from said requesting data processing system into serial data before transmitting said serial data to said crossbar switch; and

a means for converting serial data before transmitting said data frame to said destination data processing system.

9. (previously presented) The data transmission system according to Claim 8, wherein said serial data is implemented as concatenated slots of a cell size in a high-level data link control (HDLC) format.

10. (previously presented) The data transmission system according to Claim 8, wherein a plurality of request signals (REQ) are serial encoded signals of thirty-two bits.

11. (cancelled)

12. (currently amended) The data transmission system according to Claim 10, wherein a plurality of grant signals (GNT) are serially encoded signals of thirty-two bits that are sampled by a signal at the frequency of the data clock of the system multiplied by sixteen.

13. (previously presented) The data transmission system according to Claim 12, wherein said plurality of request (REQ) signals and said plurality of grant (GNT) signals both include a first pair of data bytes including sixteen bits defining a destination address of said data frame to be transmitted and a second pair of data bytes including sixteen bits carrying the connection time defined by the number of slots to be transmitted.

14. (previously presented) The data transmission system according to Claim 13, wherein said first data byte defining said destination address includes one bit for each of said plurality of adapters, a bit being set when said destination address corresponds to said destination adapter, which enables a point-to-point connection, a multicast connection or a broadcast connection.

15. (previously presented) The data transmission system according to Claim 11, wherein said serial communication controller further comprises:

a means for generating a high-level data link control (HDLC) frame, in response receiving said data frame from said requesting data processing system coupled to said requesting adapter before transmitting said HDLC frames to said crossbar switch.

16. (previously presented) The data transmission system according to Claim 15, wherein said means for generating in said serial communication controller further includes:

a means for generating a high-level data link control (HDLC) flag to start said HDLC frame;

a means for serializing a set of incoming parallel data bytes;

a means for computing a frame check sequence (FCS) after said set of incoming parallel data bytes; and

a means for generating another HDLC flag to end said HDLC frame.

17. (previously presented) The data transmission system according to Claim 16, wherein said serial communication controller further comprises:

a means for converting said high-level data link control (HDLC) frames received from said crossbar switch into a plurality of data frames to be transmitted to said destination data processing system.

18. (previously presented) The data transmission system according to Claim 17, wherein said means for converting in said serial communication controller further includes:

a means for detecting a starting high-level data link control (HDLC) frame in a incoming HDLC frame;

a means for checking the data integrity of said HDLC frame by computing a frame check sequence (FCS); and

a means for deserializing the data bits of said HDLC frame to provide a set of data bytes of said data frame.

19. (previously presented) The data transmission system according to Claim 18, wherein each of said plurality of adapters further comprises:

a memory divided into at least two independent areas, a first data processing system-to-switch area organized in a first plurality of buffers for storing at least said data frame received from a data processing system coupled to said adapter and to be transmitted to another data processing system, and a second switch-to-data processing system area organized in a second plurality of buffers for storing at least said data frame received from another data processing system and to be transmitted to said data processing system coupled to said adapter.

20. (previously presented) The data transmission system according to Claim 19, wherein each of said plurality of adapters further comprises:

a controller, for converting a serial data frame to a parallel data frame, or for converting a parallel data frame to a serial data frame.

21. (previously presented) The data transmission system according to Claim 20, wherein said controller comprises:

a means for synchronizing a clock during a set of preamble bytes when receiving said data frame;

a means for detecting an incoming data frame through a delimiter byte of said frame;

a means for checking data integrity of said data frame by computing a frame check sequence (FCS) bytes;

a means for removing a set of protocol information of said data frame; and

a means for deserializing the remaining incoming bits of said data frame to provide parallel data bytes.

22. (previously presented) The data transmission system according to Claim 20, wherein said controller further includes:

a means for serializing incoming data bytes received from said serial communication controller;

a means for generating protocol information bytes to be included in said data frame; and

a means for computing said frame check sequence (FCS) of said data frame before transmitting said data frame to a data processing system connected to an adapter.

23. (previously presented) The data transmission system according to Claim 22, further comprises:

an arbiter for taking care of the contention between requests sent from said controller and requests sent from said serial communication controller.

24. (previously presented) The data transmission system according to Claim 23, wherein said scheduler further comprises:

an algorithm means for determining which request is to be granted each time a new request (REQ) signal is received, said new REQ signal to be granted utilized as a grant (GNT) signal being transmitted to said requesting LAN adapter; and

a control logic means, further including:

a memory for storing said request (REQ) signal received from said requesting adapter.